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(54) **ORGANIC LIGHT EMITTING DIODE DISPLAY**

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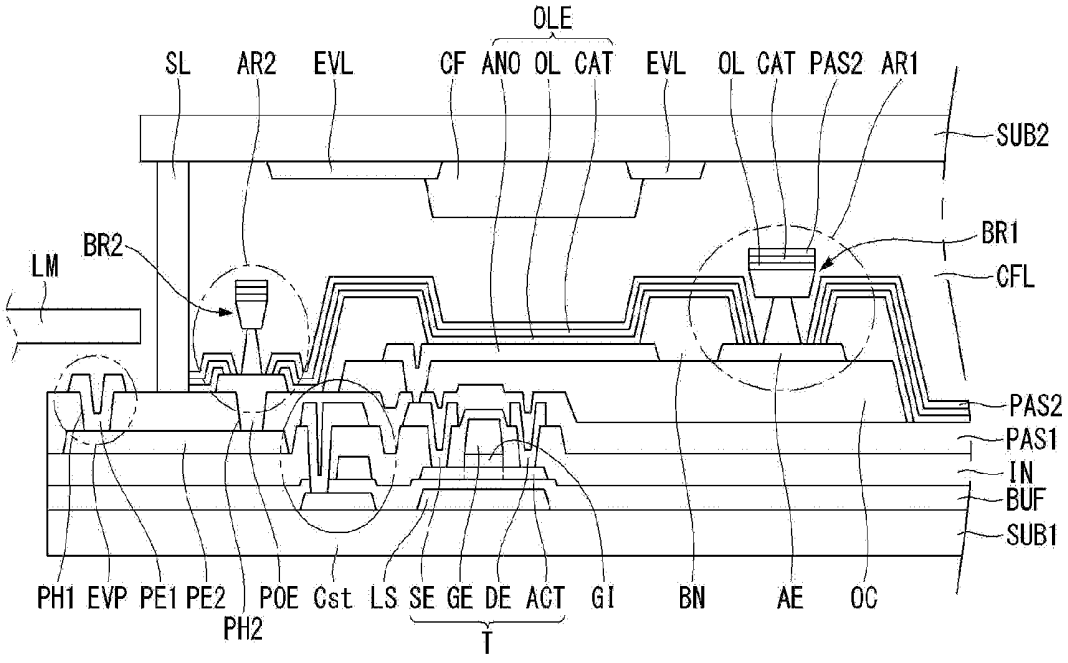
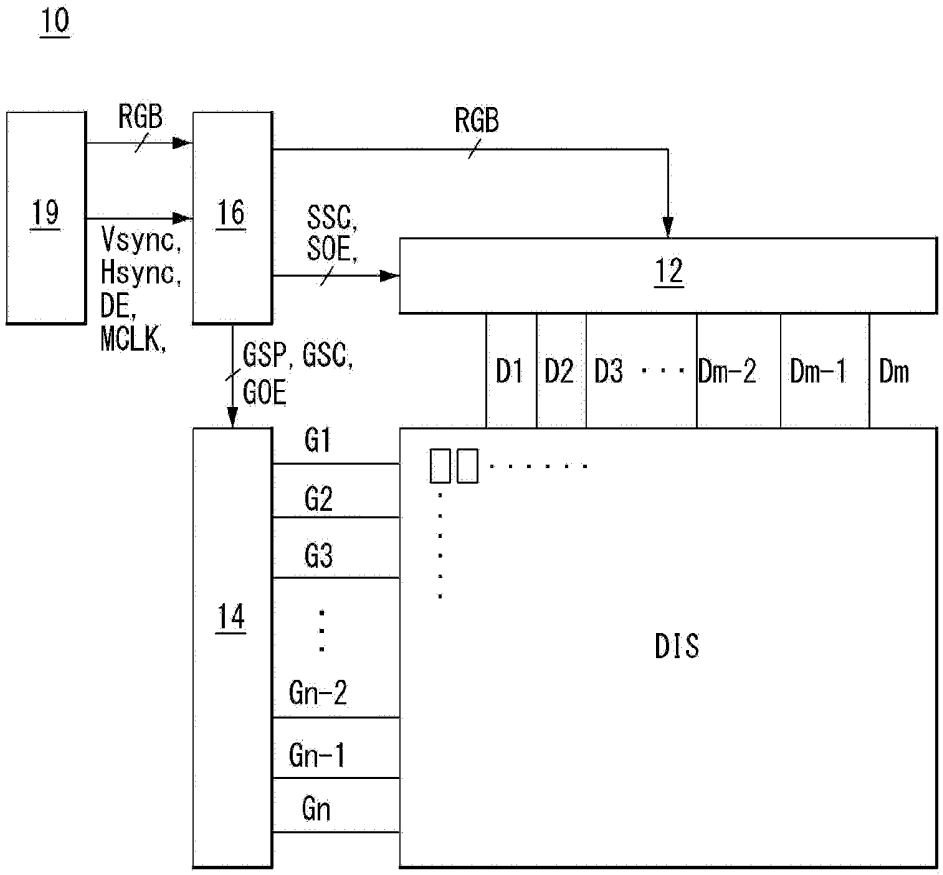
(57) **ABSTRACT**

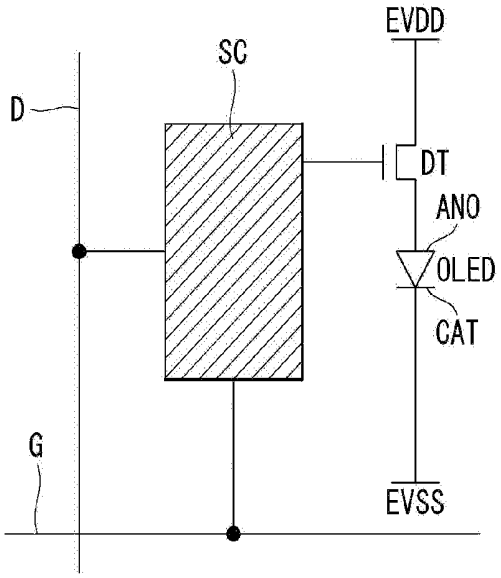
An organic light emitting diode display is disclosed. The organic light emitting diode display includes a first substrate on which pixels each including an organic light emitting diode are disposed, a second substrate including a power line supplied with a power voltage and facing the first substrate, and a conductive filler layer interposed between the first substrate and the second substrate and including a conductive medium. The first substrate includes an auxiliary electrode, a first barrier disposed on the auxiliary electrode, a cathode divided by the first barrier and exposing at least a portion of the auxiliary electrode, and a protective layer disposed on the cathode, divided by the first barrier, and exposing at least a portion of the auxiliary electrode. One end of the cathode directly contacts the auxiliary electrode.



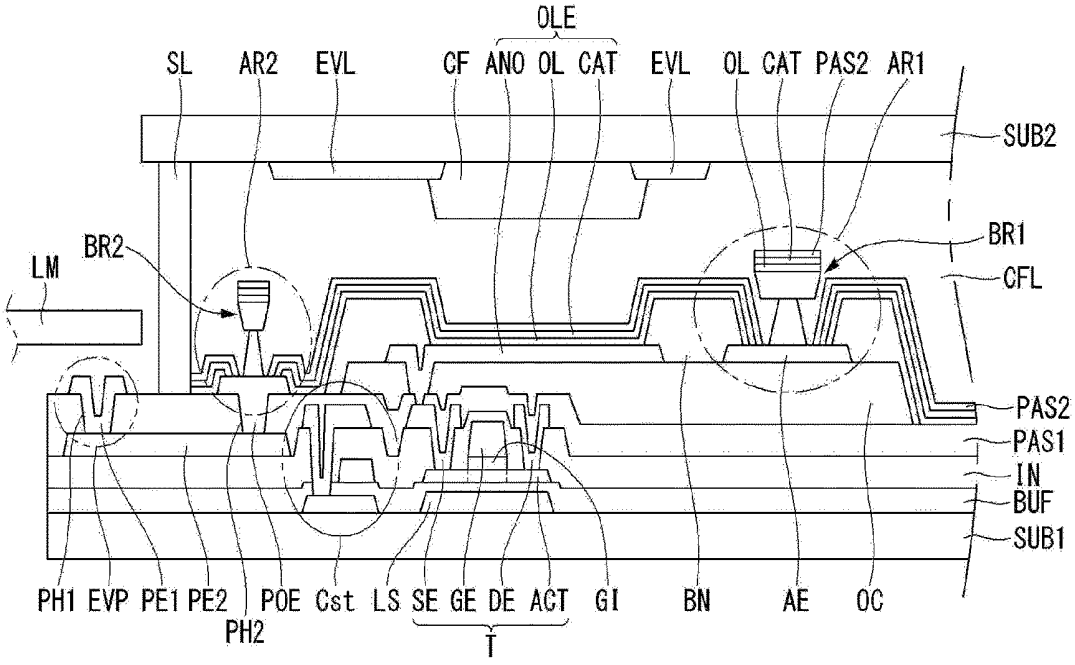
# FIG. 1


10
19
RGB
Vsync,
Hsync,
DE,
MCLK,
16
RGB
SSC,
SOE,
12
GSP, GSC,
GOE
D1
D2
D3 · · ·
Dm-2
Dm-1
Dm
14
G1
G2
G3
Gn-2
Gn-1
Gn
DIS

# FIG. 2



# FIG. 3


OLE
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CAT
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PAS2
PAS1
IN
BUF
SUB1
PH1
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AE
OC

FIG. 4

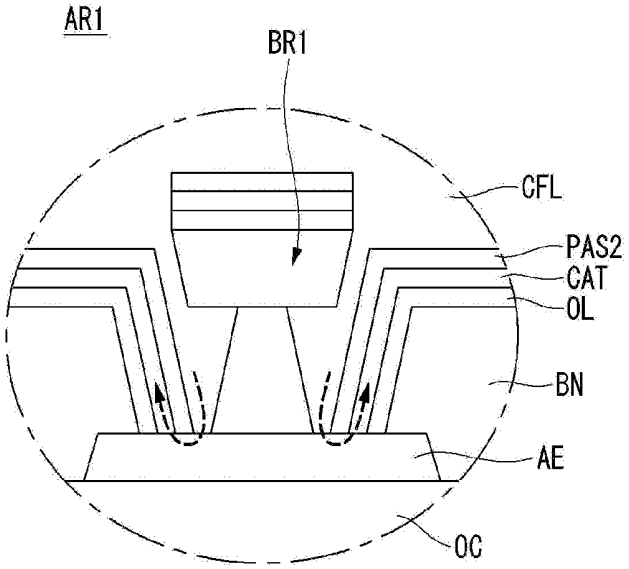
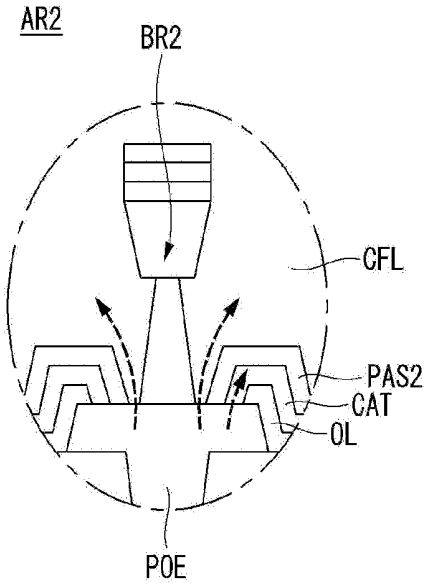
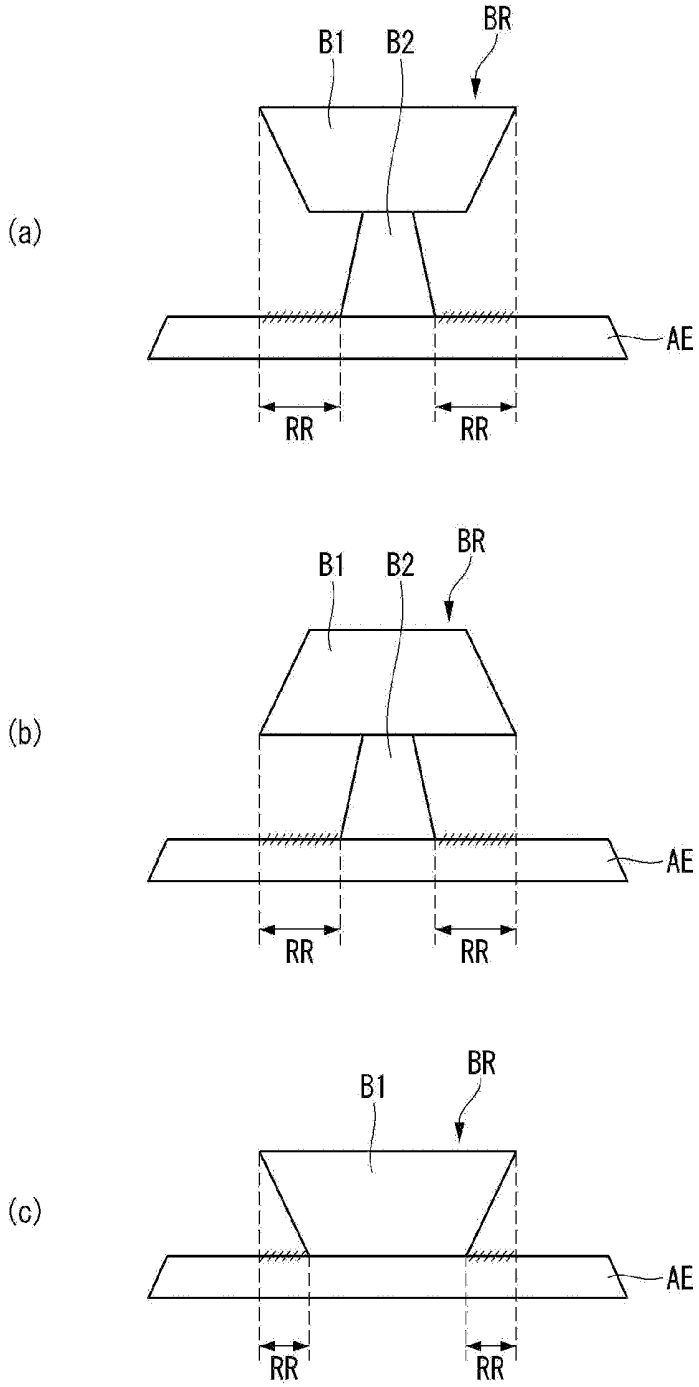


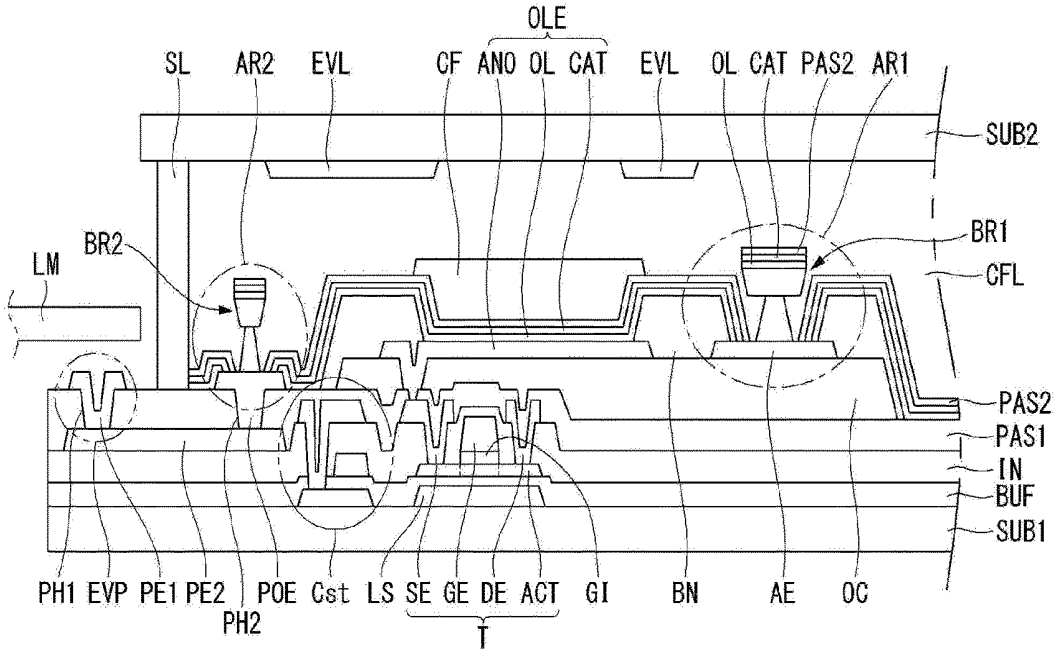

FIG. 5



# FIG. 6



# FIG. 7


OLE
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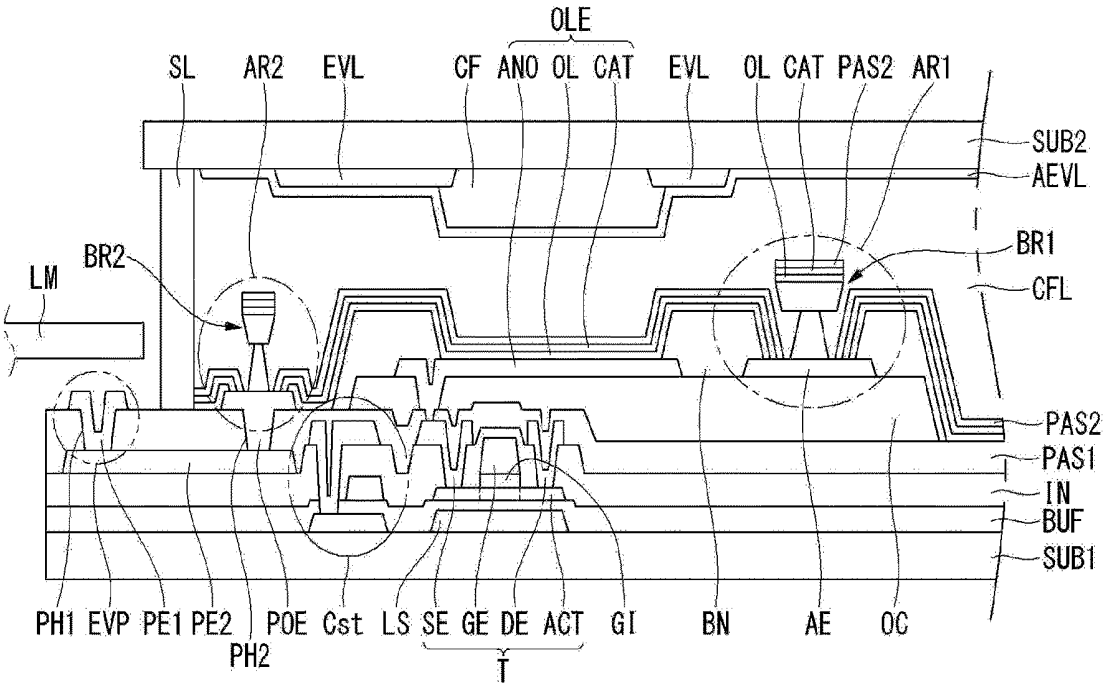
# FIG. 8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CFL
LM
BR2
PAS2
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IN
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SUB1
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POE
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# ORGANIC LIGHT EMITTING DIODE DISPLAY

## CROSS REFERENCE TO RELATED APPLICATION

**[0001]** This application claims the priority benefit of Korean Patent Application No. 10-2017-0118618 filed on Sep. 15, 2017, which is incorporated herein by reference in its entirety for all purposes as if fully set forth herein.

## BACKGROUND

### Field of the Disclosure

**[0002]** The present disclosure relates to a display device, and more particularly, to an organic light emitting diode display. Although the present disclosure is suitable for a wide scope of applications, it is particularly suitable for minimizing a variation in a low potential power voltage on a different position to achieve a uniform luminance in the organic light emitting diode display

### Description of the Background

**[0003]** Various display devices have replaced heavier and larger cathode ray tubes (CRTs). Such display devices include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), and an organic light emitting diode (OLED) display.

**[0004]** In more detail, an OLED display is a self-emission display emits light by exciting an organic compound. The OLED display does not require a backlight unit used in a liquid crystal display and thus has advantages of a thin profile, light weight, and a simple manufacturing process. The OLED display can be also manufactured under a low temperature condition and has a fast response time of **1** ms or less, a low power consumption, a wide viewing angle, and a high contrast, etc. Thus, the OLED display has been widely used these days.

**[0005]** The OLED display includes organic light emitting diodes (OLEDs) converting electric energy into light energy. The OLED includes an anode, a cathode, and an organic emission layer between the anode and the cathode. The OLED display is configured such that the OLED emits light while excitons formed by combining holes from the anode and electrons from the cathode inside an emission layer fall from an excited state to a ground state, and thus displays an image.

**[0006]** However, a large-area OLED display cannot maintain a uniform luminance throughout the entire surface of an active area, on which an input image is displayed, and can cause a luminance variation (or deviation) on different positions. More specifically, a cathode constituting an organic light emitting diode is formed to cover most of the active area, and there is a problem that a power voltage applied to the cathode cannot have a constant voltage value throughout the entire surface of the active area. For example, as a difference between a voltage value at an entrance of the cathode supplied with the power voltage and a voltage value at a position apart from the entrance increases due to a resistance of the cathode, the luminance variation depending on the position increases.

**[0007]** Generally, there is more problematic in a top emission type display device. Namely, in the top emission type display device, because it is necessary to secure a transmittance of a cathode positioned at an upper layer of an organic light emitting diode, the cathode is formed of a transparent conductive material such as indium tin oxide (ITO) and an opaque conductive material with a very thin thickness. In this instance, because a surface resistance of the cathode increases, a luminance variation depending on a position greatly increases corresponding to an increase in the surface resistance.

**[0008]** In order to solve such a problem, a method was proposed to prevent a voltage drop depending on a position by forming a low potential power voltage line including a low resistance material and connecting the low potential power voltage line to a cathode. In the proposed method according to the related art, because the low potential power voltage line was formed on a lower substrate including transistors, one pixel has to further include a connection area of the low potential power voltage line and the cathode in addition to a thin film transistor area and a storage capacitor area. Thus, it was difficult to apply the related art to a high-resolution display including small-sized unit pixels.

## SUMMARY

**[0009]** The present disclosure provides an organic light emitting diode display capable of achieving a uniform luminance by minimizing a variation in a low potential power voltage depending on a position.

**[0010]** In one aspect, there is provided an organic light emitting diode display comprising a first substrate on which pixels each including an organic light emitting diode are disposed, a second substrate including a power line supplied with a power voltage, the second substrate facing the first substrate, and a conductive filler layer interposed between the first substrate and the second substrate, the conductive filler layer including a conductive medium, wherein the first substrate includes an auxiliary electrode, a first barrier disposed on the auxiliary electrode, a cathode included in the organic light emitting diode and divided by the first barrier, the cathode exposing at least a portion of the auxiliary electrode, and one end of the cathode directly contacting the auxiliary electrode, and a protective layer disposed on the cathode and divided by the first barrier, the protective layer exposing at least a portion of the auxiliary electrode, wherein the cathode is electrically connected to the power line through the conductive filler layer and the exposed portion of the auxiliary electrode.

**[0011]** In another aspect, there is provided an organic light emitting diode display including first and second substrates facing each other, a plurality of pixels defined at the first substrate and each pixel having an organic light emitting diode, comprising an auxiliary electrode at the first substrate a first barrier disposed on the auxiliary electrode; a conductive filler layer disposed between the first and second substrates and including a conductive medium; a power line supplied with a power voltage at the second substrate; a cathode included in the organic light emitting diode and divided by the first barrier, wherein the cathode exposes a portion of the auxiliary electrode, one end of the cathode directly contacts the auxiliary electrode, and is electrically connected to the power line through the conductive filler layer; and a protective layer disposed on the cathode and divided by the first barrier and exposing a portion of the auxiliary electrode.

**[0012]** In a further aspect, there is provided an organic light emitting diode display including first and second

substrates facing each other, a plurality of pixels defined at the first substrate and each pixel having an organic light emitting diode, comprising an auxiliary electrode at the first substrate; a first barrier disposed on the auxiliary electrode; a conductive filler layer disposed between the first and second substrates and including a conductive medium; a power line supplied with a power voltage at the second substrate; a cathode included in the organic light emitting diode and divided by the first barrier, wherein the cathode exposes a portion of the auxiliary electrode, one end of the cathode directly contacts the auxiliary electrode, and is electrically connected to the power line through the conductive filler layer; and a protective layer disposed on the cathode and divided by the first barrier and exposing a portion of the auxiliary electrode, a sealant disposed at an edge of the first substrate and an edge of the second substrate and accommodating the conductive filler layer with the first and second substrates; a power electrode disposed at the first substrate and inside the sealant; and a second barrier disposed on the power electrode and dividing the cathode that exposes a portion of the power electrode.

**[0013]** The organic light emitting diode display further comprises a sealant disposed at an edge of the first substrate and an edge of the second substrate, the conductive filler layer being accommodated inside the sealant, a power electrode disposed on the first substrate and inside the sealant, and a second barrier disposed on the power electrode. The cathode is divided by the second barrier and exposes at least a portion of the power electrode. The protective layer is divided by the second barrier and exposes at least a portion of the power electrode. The power electrode is electrically connected to the power line through the conductive filler layer.

**[0014]** One end of the cathode directly contacts the power electrode.

**[0015]** The organic light emitting diode display further comprises a connection member disposed outside the sealant and connected to the first substrate. The first substrate further includes a power pad that is connected to the connection member, is supplied with the power voltage through the connection member, and transfers the power voltage to the power electrode.

**[0016]** Each of the first substrate and the second substrate includes an emission region, to which light from the organic light emitting diode is emitted, and a non-emission region outside the emission region. The power line is disposed in the non-emission region.

**[0017]** The second substrate further includes an auxiliary power line, of which one surface directly contacts the power line, and another surface opposite the one surface directly contacts the conductive filler layer. The auxiliary power line has an area larger than the power line and includes a transparent conductive material.

**[0018]** The first barrier includes a first structure disposed on a second structure. An edge of the first structure protrudes from an edge of the second structure to the outside by a predetermined distance.

**[0019]** The first barrier has a shape in which an edge of an upper side protrudes from an edge of a lower side to the outside by a predetermined distance.

**[0020]** The second substrate further includes color filters respectively assigned to the pixels. The color filters are partitioned by the power line.

**[0021]** The first substrate further includes color filters respectively assigned to the pixels. The color filters are disposed on the cathode or on the protective layer.

**[0022]** The power line includes a low resistance material.

**[0023]** The organic light emitting diode display further comprises an organic light emitting layer included in the organic light emitting diode and divided by the first barrier, the organic light emitting layer exposing at least a portion of the auxiliary electrode. On the auxiliary electrode, the cathode is extended further than the organic light emitting layer.

**[0024]** A portion of the cathode and a portion of the protective layer are sequentially stacked on the first barrier.

**[0025]** The conductive filler layer includes at least one of poly(3,4-ethylenedioxythiophene) (PEDOT) which is a conductive polymer, and an ionic liquid.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0026]** The accompanying drawings, that may be included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this application, illustrate aspects of the disclosure and together with the description serve to explain various principles of the disclosure.

**[0027]** In the drawings:

**[0028]** FIG. **1** is a block diagram schematically illustrating an organic light emitting diode (OLED) display according to an aspect of the present disclosure;

**[0029]** FIG. **2** schematically illustrates configuration of a pixel shown in FIG. **1**;

**[0030]** FIG. **3** is a cross-sectional view of an OLED display according to a first aspect of the disclosure;

**[0031]** FIG. **4** is an enlarged view of an area AR**1** shown in FIG. **3**;

**[0032]** FIG. **5** is an enlarged view of an area AR**2** shown in FIG. **3**;

**[0033]** FIG. **6** is cross-sectional views schematically illustrating a shape of a barrier including first and second barriers;

**[0034]** FIG. **7** is a cross-sectional view of an OLED display according to a second aspect of the disclosure; and

**[0035]** FIG. **8** is a cross-sectional view of an OLED display according to a third aspect of the disclosure.

## DETAILED DESCRIPTION

**[0036]** Reference will now be made in detail to aspects of the disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts. Detailed descriptions of known arts will be omitted if such may mislead the aspects of the disclosure. In describing various aspects, the same components may be described in a first aspect, and a description thereof may be omitted in other aspects.

**[0037]** The terms "first", "second", etc. may be used to describe various components, but the components are not limited by such terms. The terms are used only for the purpose of distinguishing one component from other components.

**[0038]** FIG. **1** is a block diagram schematically illustrating an organic light emitting diode (OLED) display according to an aspect of the present disclosure. FIG. **2** schematically illustrates configuration of a pixel shown in FIG. **1**.

**[0039]** Referring to FIG. **1**, an OLED display **10** according to an aspect of the disclosure includes a display driving circuit and a display panel DIS.

**[0040]** The display driving circuit includes a data driving circuit **12**, a gate driving circuit **14**, and a timing controller **16**. The display driving circuit supplies a video data voltage of an input image to a plurality of pixels of the display panel DIS. The data driving circuit **12** converts digital video data RGB received from the timing controller **16** into an analog gamma compensation voltage and generates a data voltage. The data voltage output from the data driving circuit **12** is supplied to data lines D**1** to Dm, where m is a positive integer. The gate driving circuit **14** sequentially supplies a gate signal synchronized with the data voltage to gate lines G**1** to Gn and selects pixels of the display panel DIS to which the data voltage is applied, where n is a positive integer.

**[0041]** The timing controller **16** receives timing signals, such as a vertical sync signal Vsync, a horizontal sync signal Hsync, a data enable signal DE, and a main clock MCLK, from a host system **19** and synchronizes operation timing of the data driving circuit **12** with operation timing of the gate driving circuit **14**. A data timing control signal for controlling the data driving circuit **12** includes a source sampling clock SSC, a source output enable signal SOE, and the like. A gate timing control signal for controlling the gate driving circuit **14** includes a gate start pulse GSP, a gate shift clock GSC, a gate output enable signal GOE, and the like.

**[0042]** The host system **19** may be one of a television system, a set-top box, a navigation system, a DVD player, a Blu-ray player, a personal computer (PC), a home theater system, a phone system, and other systems that include or operate in conjunction with a display. The host system **19** includes a system-on chip (SoC), in which a scaler is embedded, and converts the digital video data RGB of the input image into a format suitable for displaying the input image on the display panel DIS. The host system **19** transmits the digital video data RGB of the input image and the timing signals Vsync, Hsync, DE and MCLK to the timing controller **16**.

**[0043]** The display panel DIS includes a pixel array. The pixel array includes the pixels defined by the data lines D**1** to Dm and the gate lines G**1** to Gn. Each pixel includes an organic light emitting diode (OLED) serving as a self-emission element.

**[0044]** Referring to FIG. **2**, the display panel DIS includes a plurality of data lines D, a plurality of gate lines G intersecting the data lines D, and a plurality of pixels respectively arranged at intersections of the data lines D and the gate lines G in a matrix form. Each pixel includes an OLED, a driving thin film transistor (TFT) DT for controlling an amount of current flowing through the OLED, and a programming unit SC for setting a gate-to-source voltage of the driving TFT DT.

**[0045]** The programming unit SC may include at least one switching TFT and at least one storage capacitor. The switching TFT is turned on in response to a gate signal from the gate line G to thereby apply a data voltage from the data line D to one electrode of the storage capacitor. The driving TFT DT controls an amount of current supplied to the OLED depending on a magnitude of voltage stored in the storage capacitor, thereby controlling an amount of light emitted by the OLED. The amount of light emitted by the OLED is proportional to the amount of current supplied from the driving TFT DT. The pixel is connected to a high potential power voltage source and a low potential power voltage source and receives a high potential power voltage EVDD and a low potential power voltage EVSS from a power generator (not shown). The TFTs constituting the pixel may be p-type TFTs or n-type TFTs. Further, semiconductor layers of the TFTs constituting the pixel may include amorphous silicon, polycrystalline silicon, or oxide. In the following description, aspects of the disclosure use a semiconductor layer including oxide as an example. The OLED includes an anode ANO, a cathode CAT, and an organic light emitting layer between the anode ANO and the cathode CAT. The anode ANO is connected to the driving TFT DT.

**[0046]** FIG. **3** is a cross-sectional view of an OLED display according to a first aspect of the disclosure. FIG. **4** is an enlarged view of an area AR**1** shown in FIG. **3**.

**[0047]** Referring to FIG. **3**, an OLED display according to a first aspect of the disclosure includes a display panel including a first substrate SUB**1** and a second substrate SUB**2** facing each other and a conductive filler layer CFL between the first substrate SUB**1** and the second substrate SUB**2**. The first substrate SUB**1** is a thin film transistor array substrate on which a thin film transistor T and an organic light emitting diode OLE are disposed. The second substrate SUB**2** is a substrate on which a low potential power voltage line (hereinafter referred to as "Evss line") EVL is disposed. The second substrate SUB**2** may function as an encapsulation substrate. The first substrate SUB**1** and the second substrate SUB**2** may be attached to each other by using a sealant SL. The sealant SL is disposed at an edge of the first substrate SUB**1** and an edge of the second substrate SUB**2** and maintains a predetermined distance (or gap) between the first substrate SUB**1** and the second substrate SUB**2**. The conductive filler layer CFL may be disposed inside the sealant SL.

**[0048]** The first substrate SUB**1** may be made of a glass material or a plastic material. For example, the first substrate SUB**1** may be made of a plastic material such as polyimide (PI), polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polycarbonate (PC) and may have flexible characteristics.

**[0049]** The thin film transistor T and the organic light emitting diode OLE connected to the thin film transistor T are formed on the first substrate SUB**1**. A light shielding layer LS and a buffer layer BUF may be formed between the first substrate SUB**1** and the thin film transistor T. The light shielding layer LS is disposed to overlap a semiconductor layer, particularly, a channel of the thin film transistor T and can protect an oxide semiconductor element from external light. The buffer layer BUF can block ions or impurities diffused from the first substrate SUB**1** and also block moisture penetration from the outside.

**[0050]** The thin film transistor T includes a semiconductor layer ACT, a gate electrode GE, a source electrode SE, and a drain electrode DE.

**[0051]** A gate insulating layer GI and the gate electrode GE are disposed on the semiconductor layer ACT. The gate insulating layer GI functions to insulate the gate electrode GE and may be formed of silicon oxide (SiOx). However, aspects are not limited thereto. The gate electrode GE is disposed to overlap the semiconductor layer ACT with the gate insulating layer GI interposed therebetween. The gate electrode GE may be formed as a single layer or a multilayer of copper (Cu), molybdenum (Mo), aluminum (Al), chrome

(Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), tantalum (Ta), tungsten (W), or a combination thereof. The gate insulating layer GI and the gate electrode GE may be patterned using the same mask. In this instance, the gate insulating layer GI and the gate electrode GE may have the same area. Although not shown, the gate insulating layer GI may be formed to cover the entire surface of the first substrate SUB**1**.

**[0052]** An interlayer dielectric layer IN is positioned on the gate electrode GE. The interlayer dielectric layer IN functions to insulate the gate electrode GE and the source and drain electrodes SE and DE from each other. The interlayer dielectric layer IN may be formed of silicon oxide (SiOx), silicon nitride (SiNx), or a multilayer thereof. However, aspects are not limited thereto.

**[0053]** The source electrode SE and the drain electrode DE are positioned on the interlayer dielectric layer IN. The source electrode SE and the drain electrode DE are spaced from each other by a predetermined distance. The source electrode SE contacts one side of the semiconductor layer ACT through a source contact hole penetrating the interlayer dielectric layer IN. The drain electrode DE contacts the other side of the semiconductor layer ACT through a drain contact hole penetrating the interlayer dielectric layer IN.

**[0054]** Each of the source electrode SE and the drain electrode DE may be formed as a single layer or as a multilayer. When each of the source electrode SE and the drain electrode DE is formed as a single layer, each of the source electrode SE and the drain electrode DE may be formed of molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), or a combination thereof. When each of the source electrode SE and the drain electrode DE is formed as a multilayer, each of the source electrode SE and the drain electrode DE may be formed as a double layer of Mo/Al—Nd, Mo/Al, Ti/**A1** or Cu/MoTi, or as a triple layer of Mo/Al—Nd/Mo, Mo/Al/Mo, Ti/Al/Ti or MoTi/Cu/MoTi.

**[0055]** A passivation layer PAS**1** is positioned on the thin film transistor T. The passivation layer PAS**1** protects the thin film transistor T and may be formed of silicon oxide (SiOx), silicon nitride (SiNx), or a multilayer thereof.

**[0056]** A planarization layer OC is positioned on the passivation layer PAS**1**. The planarization layer OC can reduce or planarize a height difference (or step coverage) of an underlying structure and may be formed of an organic material such as photo acryl, polyimide, benzocyclobutene-based resin, and acrylate-based resin. If necessary or desired, one of the passivation layer PAS**1** and the planarization layer OC can be omitted.

**[0057]** The organic light emitting diode OLE and an auxiliary electrode AE are positioned on the planarization layer OC. The organic light emitting diode OLE includes an anode ANO, an organic light emitting layer OL, and a cathode CAT.

**[0058]** More specifically, the anode ANO is positioned on the planarization layer OC. The anode ANO is connected to the drain electrode DE of the thin film transistor T through a contact hole penetrating the passivation layer PAS**1** and the planarization layer OC. The anode ANO may include a reflective layer and thus serve as a reflective electrode. The reflective layer may be formed of aluminum (Al), copper (Cu), silver (Ag), palladium (Pd), nickel (Ni), or a combination thereof. For example, the reflective layer may be formed of Ag/Pd/Cu (APC) alloy. The anode ANO may be formed as a multilayer including a reflective layer.

**[0059]** The auxiliary electrode AE is positioned on the planarization layer OC. The auxiliary electrode AE may be formed of the same material as the anode ANO at the same layer as the anode ANO. In this instance, because a separate process for forming the auxiliary electrode AE does not need to be performed, the number of processes can be reduced. Hence, the manufacturing time and the manufacturing cost can be reduced, and product yield can be remarkably improved. As will be described later, the auxiliary electrode AE may function to receive a low potential power voltage from the Evss line EVL through the conductive filler layer CFL and transfer the low potential power voltage to the cathode CAT.

**[0060]** A bank layer BN is positioned on the first substrate SUB**1**, on which the anode ANO and the auxiliary electrode AE are formed, and partitions pixels. The bank layer BN may be formed of an organic material such as polyimide, benzocyclobutene-based resin, and acrylate. A center portion of the anode ANO exposed by the bank layer BN may be defined as an emission region.

**[0061]** The bank layer BN may be configured to expose the center portion of the anode ANO and cover an edge of the anode ANO. The exposed portion of the anode ANO may be designed to have as large an area as possible, in order to sufficiently secure an aperture ratio. Further, the bank layer BN may be configured to expose a center portion of the auxiliary electrode AE and cover an edge of the auxiliary electrode AE. The exposed portion of the auxiliary electrode AE may be designed to have as large an area as possible, in order to sufficiently secure a contact area between the auxiliary electrode AE and the conductive filler layer CFL.

**[0062]** A first barrier BR**1** is positioned on the first substrate SUB**1** on which the bank layer BN is formed. The first barrier BR**1** is positioned on the auxiliary electrode AE. The first barrier BR**1** functions to physically divide each of the organic light emitting layer OL, the cathode CAT, and a protective layer PAS**2** that will be formed later. In other words, each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS**2** is disposed on the auxiliary electrode AE and is physically divided by the first barrier BR**1**. Hence, each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS**2** may be discontinuously formed on the auxiliary electrode AE.

**[0063]** The bank layer BN and the planarization layer OC may be patterned to cover only the thin film transistor T and a storage capacitor Cst connected to the thin film transistor T inside the pixel. As shown in FIG. **3**, the storage capacitor Cst may have a triple structure in which first to third capacitor electrodes are stacked. However, aspects are not limited thereto. For example, the storage capacitor Cst may be implemented as a plurality of layers.

**[0064]** The organic light emitting layer OL is positioned on the first substrate SUB**1** on which the first barrier BR**1** is formed. The organic light emitting layer OL may be widely formed on a front surface of the first substrate SUB**1**. The organic light emitting layer OL is a layer, in which electrons and holes combine and emit light. The organic light emitting layer OL includes an emission layer EML and may further include one or more of a hole injection layer HIL, a hole transport layer HTL, an electron transport layer ETL, and an

electron injection layer EIL. The emission layer EML may include a light emitting material that generates white light.

**[0065]** The organic light emitting layer OL on the auxiliary electrode AE is physically divided by the first barrier BR1. The organic light emitting layer OL is divided by the first barrier BR1 and exposes at least a portion of the auxiliary electrode AE around the first barrier BR1. A portion of the organic light emitting layer OL divided by the first barrier BR1 is positioned on the first barrier BR1.

**[0066]** The cathode CAT is positioned on the organic light emitting layer OL. The cathode CAT may be widely formed on the front surface of the first substrate SUB1. The cathode CAT may be formed of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). Alternatively, the cathode CAT may be formed of a material, which is thin enough to transmit light, for example, magnesium (Mg), calcium (Ca), aluminum (Al), silver (Ag), or a combination thereof.

**[0067]** The cathode CAT on the auxiliary electrode AE is physically divided by the first barrier BR1. The cathode CAT is divided by the first barrier BR1 and exposes at least a portion of the auxiliary electrode AE around the first barrier BR1. A portion of the cathode CAT divided by the first barrier BR1 is positioned on the first barrier BR1. As will be described later, the cathode CAT may directly contact the auxiliary electrode AE and may be supplied with the low potential power voltage through the auxiliary electrode AE.

**[0068]** The cathode CAT covers the organic light emitting layer OL, and one end of the cathode CAT directly contacts the auxiliary electrode AE. Namely, one end of the cathode CAT, which is divided by the first barrier BR1 and is exposed, directly contacts an exposed upper surface of the auxiliary electrode AE. Such a structure may be implemented by a step coverage difference between materials forming the organic light emitting layer OL and the cathode CAT. For example, because the cathode CAT is made of a transparent conductive material having better step coverage than a formation material of the organic light emitting layer OL, the cathode CAT may be configured to directly contact the auxiliary electrode AE. Furthermore, in order to implement the structure, the organic light emitting layer OL and the cathode CAT may be formed using different methods. For example, the organic light emitting layer OL may be formed using a thermal deposition method, and the cathode CAT may be formed using a sputtering method. Hence, one end of the divided cathode CAT may be extended further than one end of the divided organic light emitting layer OL and may directly contact the auxiliary electrode AE.

**[0069]** The protective layer PAS2 is positioned on the cathode CAT. The protective layer PAS2 may be widely formed on the front surface of the first substrate SUB1. The protective layer PAS2 may be formed of a material such as silicon oxide (SiOx) and silicon nitride (SiNx).

**[0070]** More specifically, the protective layer PAS2 is positioned on the cathode CAT and can block the penetration of foreign material that may enter the organic light emitting diode OLE. For example, because the cathode CAT including a transparent conductive material is a crystalline component and cannot block the penetration of ions and moisture, ionic components or external impurities of an ionic liquid included in the conductive filler layer CFL may pass through the cathode CAT and may enter the organic light emitting layer OL. The first aspect of the disclosure further includes the protective layer PAS2 on the organic light emitting diode OLE and can block the penetration of foreign material that may enter the organic light emitting diode OLE. Hence, the first aspect of the disclosure can prevent a reduction in lifespan of the organic light emitting diode OLE and a luminance reduction.

**[0071]** In addition, the protective layer PAS2 is positioned on the cathode CAT and can buffer or mitigate a stress applied to the cathode CAT when the first substrate SUB1 and the second substrate SUB2 are attached to each other. For example, because the cathode CAT including the transparent conductive material has brittle characteristics, the cathode CAT may easily crack due to an external force applied. The first aspect of the disclosure further includes the protective layer PAS2 on the cathode CAT and can prevent a crack from being generated in the cathode CAT. Furthermore, the first aspect of the disclosure can prevent the penetration of oxygen or moisture due to the crack.

**[0072]** As will be described later, the conductive filler layer CFL according to the first aspect of the disclosure may include an ionic liquid. In this instance, because the ionic liquid directly contacts the cathode CAT, the cathode CAT can be oxidized. The first aspect of the disclosure further includes the protective layer PAS2 between the cathode CAT and the conductive filler layer CFL and can prevent a problem that the cathode CAT is deteriorated.

**[0073]** The protective layer PAS2 on the auxiliary electrode AE is physically divided by the first barrier BR1. The protective layer PAS2 is divided by the first barrier BR1 and exposes at least a portion of the auxiliary electrode AE around the first barrier BR1. A portion of the protective layer PAS2 divided by the first barrier BR1 is positioned on the first barrier BR1. Hence, the portion of the organic light emitting layer OL, the portion of the cathode CAT, and the portion of the protective layer PAS2, each of which is divided by the first barrier BR1, are sequentially stacked on the first barrier BR1.

**[0074]** The Evss line EVL and a color filter CF are formed on the second substrate SUB2. A stacking order of the Evss line EVL and the color filter CF on the second substrate SUB2 may be changed. For example, the color filter CF may be formed after the Evss line EVL is formed, or the Evss line EVL may be formed after the color filter CF is formed.

**[0075]** The Evss line EVL includes a low resistance conductive material. For example, the Evss line EVL may be formed of molybdenum (Mo), aluminum (Al), chromium (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), or a combination thereof.

**[0076]** The Evss line EVL may include a low reflective conductive material. For example, the Evss line EVL is formed of the low reflective conductive material and thus can prevent visibility from being reduced by the reflection of external light. Thus, a display device according to aspects of the disclosure does not need to include a separate component for shielding (or absorbing) light incident from outside, like a polarizing film.

**[0077]** The Evss line EVL may function as a black matrix. Therefore, the Evss line EVL can prevent a defect of color mixture from occurring between neighboring pixels. The Evss line EVL may be disposed in a non-emission region so as to expose at least the emission region. Further, the first aspect of the disclosure can use the Evss line EVL as the black matrix and thus does not need to additionally perform a separate process for forming the black matrix. Therefore, the first aspect of the disclosure can further reduce the

number of processes compared to a related art structure, and thus can reduce the manufacturing time and the manufacturing cost and remarkably improve product yield.

**[0078]** The color filter CF may include red (R), blue (B), and green (G) color filters. The pixel may include subpixels emitting red, blue, and green light, and the color filters CF may be respectively assigned to the corresponding subpixels. The red, blue, and green color filters CF may be partitioned by the Evss line EVL. If necessary or desired, the pixel may further include a white (W) subpixel.

**[0079]** The conductive filler layer CFL is interposed between the first substrate SUB**1** and the second substrate SUB**2** and includes a conductive medium. The conductive filler layer CFL may be formed by dispersing conductive fillers in a solvent. Alternatively, the conductive filler layer CFL may include a conductive solvent. For example, the conductive filler layer CFL may include at least one of a conductive polymer, such as poly(3,4-ethylenedioxythiophene) (PEDOT), and an ionic liquid. However, aspects are not limited thereto.

**[0080]** The distance between the first substrate SUB**1** and the second substrate SUB**2** may be appropriately selected depending on viscosity of the conductive filler layer CFL. Because the aspect of the disclosure uses the conductive fillers having lower viscosity than non-conductive fillers, the distance between the first substrate SUB**1** and the second substrate SUB**2** can be reduced. Hence, the aspect of the disclosure can secure a wide viewing angle and a high aperture ratio.

**[0081]** The cathode CAT of the first substrate SUB**1** and the Evss line EVL of the second substrate SUB**2** are electrically connected through the conductive filler layer CFL. Thus, the low potential power voltage is applied to both the cathode CAT and the Evss line EVL.

**[0082]** More specifically, in the aspect of the disclosure, because the protective layer PAS**2** is interposed between the conductive filler layer CFL and the cathode CAT, it is difficult to bring the conductive filler layer CFL into direct contact with the cathode CAT without using the first barrier BR**1**. Referring to FIG. **4**, the aspect of the disclosure includes the first barrier BR**1** and thus can expose at least a portion of the auxiliary electrode AE while physically dividing each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS**2**. The exposed portion of the auxiliary electrode AE can directly contact the conductive filler layer CFL to receive the low potential power voltage from the Evss line EVL of the second substrate SUB**2**, and can also directly contact the cathode CAT to transfer the received low potential power voltage to the cathode CAT.

**[0083]** The first aspect of the disclosure can reduce a voltage variation (or deviation) depending on a position by connecting the Evss line EVL formed of the low resistance conductive material to the cathode CAT. Hence, the first aspect of the disclosure can reduce non-uniformity of luminance or a luminance variation.

**[0084]** The first aspect of the disclosure does not need to separately assign an area for forming the Evss line EVL and an area for connecting the Evss line EVL and the cathode CAT to the thin film transistor array substrate, as in the related art. Therefore, the first aspect of the disclosure can be easily applied to a high-resolution display having a high pixel per inch (PPI) and can remarkably improve a degree of design freedom.

**[0085]** With reference to FIG. **5**, a supply path of the low potential power voltage generated by a power generator (not shown) is described in detail below. FIG. **5** is an enlarged view of an area AR**2** shown in FIG. **3**.

**[0086]** Referring to FIGS. **3** and **5**, the OLED display according to the first aspect of the disclosure further includes a connection member LM attached to at least one side of the display panel, particularly, at least one side of the first substrate SUB**1**. The connection member LM may be a chip-on film (COF). However, aspects are not limited thereto.

**[0087]** The first substrate SUB**1** includes a low potential power voltage pad (hereinafter referred to as "Evss pad") EVP and a power electrode POE. The Evss pad EVP is disposed outside the sealant SL and is electrically connected to the connection member LM. The power electrode POE is disposed inside the sealant SL and is electrically connected to the conductive filler layer CFL.

**[0088]** The Evss pad EVP receives the low potential power voltage generated by the power generator (not shown) through the connection member LM and transfers the received low potential power voltage to the power electrode POE. The power electrode POE then transfers the low potential power voltage to the conductive filler layer CFL.

**[0089]** Namely, the connection member LM, the Evss pad EVP, the power electrode POE, the conductive filler layer CFL, and the cathode CAT may be electrically connected to form a low potential power voltage supply path, and/or the connection member LM, the Evss pad EVP, the power electrode POE, the conductive filler layer CFL, the Evss line EVL, and the cathode CAT may be electrically connected to form a low potential power voltage supply path.

**[0090]** More specifically, the Evss pad EVP includes at least one pad electrode. When a plurality of pad electrodes is used, the pad electrodes may be disposed at different layers with at least one insulating layer interposed therebetween and may be electrically connected through a pad contact hole penetrating the at least one insulating layer. For example, as shown in FIG. **3**, the Evss pad EVP may include a first pad electrode PE**1** and a second pad electrode PE**2** that are disposed at different layers with the passivation layer PAS**1** interposed therebetween, and the first pad electrode PE**1** and the second pad electrode PE**2** may be connected to each other through a first pad contact hole PHI penetrating the passivation layer PAS**1**. Hereinafter, the aspect of the disclosure describes a case where the Evss pad EVP includes the first pad electrode PE**1** and the second pad electrode PE**2** as an example, for convenience of explanation.

**[0091]** The first pad electrode PE**1** is disposed outside the sealant SL and is exposed to the outside. The exposed first pad electrode PE**1** may be attached to the connection member LM. The first pad electrode PE**1** and the connection member LM may be attached to each other through an anisotropic conductive film (ACF) layer (not shown) interposed between them.

**[0092]** The second pad electrode PE**2** is extended to the inside of the sealant SL and is electrically connected to the power electrode POE. In this instance, the second pad electrode PE**2** may contact the power electrode POE through a second pad contact hole PH**2** penetrating the passivation layer PAS**1**. FIG. **3** illustrates that the second pad electrode PE**2** and the power electrode POE are disposed with only the passivation layer PAS**1** interposed therebetween, by way of example. However, aspects are not limited thereto. For

example, the second pad electrode PE2 and the power electrode POE may be disposed at different layers with the passivation layer PAS1 and the planarization layer OC interposed therebetween and may be electrically connected to each other through a contact hole penetrating the passivation layer PAS1 and the planarization layer OC.

**[0093]** The power electrode POE may be formed together when the anode ANO is formed. Namely, the power electrode POE may be formed of the same material as the anode ANO and the auxiliary electrode AE. However, aspects are not limited thereto.

**[0094]** A second barrier BR2 is positioned on the power electrode POE. The second barrier BR2 may be formed together when the first barrier BR1 is formed. Namely, the second barrier BR2 may be formed of the same material as the first barrier BR1 and may have the same shape as the first barrier BR1. The second barrier BR2 functions to physically divide each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2. In other words, each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2 is disposed on the auxiliary electrode AE and is physically divided by the second barrier BR2. Hence, each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2 may be discontinuously formed on the auxiliary electrode AE.

**[0095]** In the aspect of the disclosure, the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2 are disposed inside the sealant SL and on the entire surface of the first substrate SUB1. Therefore, when the second barrier BR2 is not included, the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2 are formed to completely cover the power electrode POE positioned inside the sealant SL. In this instance, the power electrode POE and the cathode CAT cannot be electrically connected to each other because of the organic light emitting layer OL, and the power electrode POE and the conductive filler layer CFL cannot be electrically connected to each other because of the organic light emitting layer OL and the protective layer PAS2.

**[0096]** The first aspect of the disclosure forms the second barrier BR2 on the power electrode POE and thus can expose at least a portion of the power electrode POE while physically dividing each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2 on the power electrode POE. A portion of the organic light emitting layer OL, a portion of the cathode CAT, and a portion of the protective layer PAS2, each of which is divided by the second barrier BR2, are sequentially stacked on the second barrier BR2.

**[0097]** An exposed portion of the power electrode POE directly contacts the conductive filler layer CFL and supplies the low potential power voltage to the conductive filler layer CFL. Hence, a power supply path connecting the connection member LM, the Evss pad EVP, and the conductive filler layer CFL may be formed.

**[0098]** The cathode CAT on the power electrode POE may cover the organic light emitting layer OL, and one end of the cathode CAT may directly contact the power electrode POE. Namely, one end of the cathode CAT, which is divided by the second barrier BR2 and is exposed, may directly contact an exposed upper surface of the power electrode POE. Hence, a power supply path connecting the connection member LM, the Evss pad EVP, and the cathode CAT may be formed.

**[0099]** With reference to FIG. **6**, an example of a shape of a barrier according to an aspect of the disclosure is described below. FIG. **6** is cross-sectional views schematically illustrating a shape of a barrier including first and second barriers.

**[0100]** A barrier BR may be formed as a double layer including a first structure B1 and a second structural B2. The first structure B1 may be disposed on the second structural B2, and an edge of the first structure B1 may have an eaves shape. Namely, the edge of the first structure B1 may protrude from an edge of the second structural B2 to the outside by a predetermined distance RR. The distance RR between the edge of the first structure B1 and the edge of the second structural B2 may be properly selected so that the barrier BR can expose at least a portion of an auxiliary electrode AE while dividing each of an organic light emitting layer, a cathode, and a protective layer. In other words, each of the organic light emitting layer OL (see FIG. **3**), the cathode CAT (see FIG. **3**), and the protective layer PAS2 (see FIG. **3**) is patterned to expose at least a portion of the auxiliary electrode AE while being divided around the barrier BR due to the predetermined distance RR between the edge of the first structure B1 and the edge of the second structural B2. The first structure B1 may have a reverse taper shape as shown in (a) of FIG. **6** and may have a taper shape as shown in (b) of FIG. **6**. The first structure B1 and the second structural B2 may be formed of different materials.

**[0101]** A barrier BR may be formed as a single layer including a first structure Bl. In this instance, the first structure B1 has a shape in which an edge of an upper side protrudes from an edge of a lower side to the outside by a predetermined distance RR. For example, the first structure B1 may have a reverse taper shape as shown in (c) of FIG. **6**. Namely, a vertical cross-sectional shape of the first structure B1 may have a trapezoidal shape, the upper side may have a length longer than the lower side, and one end of the upper side may protrude from one end of the lower side to the outside by the predetermined distance RR. The distance RR between one end of the upper side and one end of the lower side may be properly selected so that the barrier BR can expose at least a portion of an auxiliary electrode AE while dividing each of an organic light emitting layer, a cathode, and a protective layer. In other words, each of the organic light emitting layer OL (see FIG. **3**), the cathode CAT (see FIG. **3**), and the protective layer PAS2 (see FIG. **3**) is patterned to expose at least a portion of the auxiliary electrode AE while being divided around the barrier BR due to the distance RR between one end of the upper side and one end of the lower side.

**[0102]** FIG. **7** is a cross-sectional view of an OLED display according to a second aspect of the disclosure. Description of structures and components identical or equivalent to those illustrated in the first aspect is omitted in the second aspect.

**[0103]** Referring to FIG. **7**, an OLED display according to a second aspect of the disclosure includes a display panel including a first substrate SUB1 and a second substrate SUB2 facing each other and a conductive filler layer CFL between the first substrate SUB1 and the second substrate SUB2. The first substrate SUB1 is a thin film transistor array substrate on which a thin film transistor T and an organic light emitting diode OLE connected to the thin film transistor T are formed. The second substrate SUB2 is a substrate on which an Evss line EVL is formed.

**[0104]** Unlike the first aspect, a color filter CF according to the second aspect of the disclosure is formed on the first substrate SUB**1**. Namely, the thin film transistor T and the organic light emitting diode OLE connected to the thin film transistor T are formed on the first substrate SUB**1**, and the color filter CF is formed on the organic light emitting diode OLE. The color filter CF may be disposed on a cathode CAT constituting the organic light emitting diode OLE or a protective layer PAS**2**. The second aspect of the disclosure can further reduce a distance between the color filter CF and an organic light emitting layer OL compared to the first aspect, and thus can increase a viewing angle and sufficiently secure an aperture ratio.

**[0105]** FIG. **8** is a cross-sectional view of an OLED display according to a third aspect of the disclosure. Description of structures and components identical or equivalent to those illustrated in the first aspect is omitted in the third aspect.

**[0106]** Referring to FIG. **8**, an OLED display according to a third aspect of the disclosure includes a display panel including a first substrate SUB**1** and a second substrate SUB**2** facing each other and a conductive filler layer CFL between the first substrate SUB**1** and the second substrate SUB**2**. The first substrate SUB**1** is a thin film transistor array substrate on which a thin film transistor T and an organic light emitting diode OLE connected to the thin film transistor T are formed. The second substrate SUB**2** is a substrate on which an Evss line EVL is formed.

**[0107]** The Evss line EVL and an auxiliary Evss line (or referred to as "auxiliary power line") AEVL are formed on the second substrate SUB**2**. A color filter CF may be positioned on the second substrate SUB**2** as in the first aspect and may be positioned on the first substrate SUB**1** as in the second aspect.

**[0108]** One surface of the auxiliary Evss line AEVL directly contacts the Evss line EVL, and the other surface of the auxiliary Evss line AEVL directly contacts the conductive filler layer CFL. The auxiliary Evss line AEVL is a power line for increasing a contact area between the Evss line EVL and the conductive filler layer CFL and may have an area larger than the Evss line EVL. The auxiliary Evss line AEVL may be interposed between the Evss line EVL and the conductive filler layer CFL. The auxiliary Evss line AEVL may be formed to cover the Evss line EVL and the color filter CF and may be widely formed on a front surface of the second substrate SUB**2** including an emission region. The auxiliary Evss line AEVL may be formed of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO).

**[0109]** Because the third aspect of the disclosure can sufficiently secure the contact area between the Evss line EVL and the conductive filler layer CFL using the auxiliary Evss line AEVL, the third aspect of the disclosure can minimize a contact failure between the Evss line EVL and the conductive filler layer CFL. Further, the third aspect of the disclosure can more efficiently reduce a voltage variation depending on a position and thus can reduce non-uniformity of luminance or a luminance variation.

**[0110]** Although the aspects have been described with reference to a number of illustrative aspects thereof, numerous other modifications and aspects may be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. In particular, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

What is claimed is:

**1**. An organic light emitting diode display comprising:
- a first substrate on which a plurality of pixels each including an organic light emitting diode are disposed;
- a second substrate including a power line supplied with a power voltage and facing the first substrate; and
- a conductive filler layer interposed between the first substrate and the second substrate and including a conductive medium,
- wherein the first substrate includes:
- an auxiliary electrode;
- a first barrier disposed on the auxiliary electrode;
- a cathode included in the organic light emitting diode and divided by the first barrier, the cathode exposing a portion of the auxiliary electrode, and one end of the cathode directly contacting the auxiliary electrode; and
- a protective layer disposed on the cathode and divided by the first barrier, the protective layer exposing a portion of the auxiliary electrode,
- wherein the cathode is electrically connected to the power line through the conductive filler layer and the exposed portion of the auxiliary electrode.

**2**. The organic light emitting diode display of claim **1**, further comprising:
- a sealant disposed at an edge of the first substrate and an edge of the second substrate and accommodating the conductive filler layer with the first and second substrates;
- a power electrode disposed at the first substrate and inside the sealant; and
- a second barrier disposed on the power electrode,
- wherein the cathode is divided by the second barrier and exposes a portion of the power electrode.

**3**. The organic light emitting diode display of claim **2**, wherein the protective layer is divided by the second barrier and exposes a portion of the power electrode and the power electrode is electrically connected to the power line through the conductive filler layer.

**4**. The organic light emitting diode display of claim **2**, wherein one end of the cathode directly contacts the power electrode.

**5**. The organic light emitting diode display of claim **2**, further comprising a connection member disposed outside the sealant and connected to the first substrate,
- wherein the first substrate further includes a power pad that is connected to the connection member, is supplied with the power voltage through the connection member, and transfers the power voltage to the power electrode.

**6**. The organic light emitting diode display of claim **1**, wherein each of the first substrate and the second substrate includes an emission region, to which light from the organic light emitting diode is emitted, and a non-emission region outside the emission region,
- wherein the power line is disposed in the non-emission region.

**7**. The organic light emitting diode display of claim **1**, wherein the second substrate further includes an auxiliary power line, of which a first surface directly contacts the

power line, and a second surface opposite the first surface directly contacts the conductive filler layer,

wherein the auxiliary power line has an area larger than the power line and includes a transparent conductive material.

**8**. The organic light emitting diode display of claim **1**, wherein the first barrier includes a first structure disposed on a second structure,

wherein an edge of the first structure protrudes from an edge of the second structure to the outside by a predetermined distance.

**9**. The organic light emitting diode display of claim **1**, wherein the first barrier has a shape in which an edge of an upper side protrudes from an edge of a lower side.

**10**. The organic light emitting diode display of claim **1**, wherein the second substrate further includes a plurality of color filters corresponding to the plurality of pixels,

wherein the color filters are partitioned by the power line.

**11**. The organic light emitting diode display of claim **1**, wherein the first substrate further includes a plurality of color filters corresponding to the plurality of pixels,

wherein the color filters are disposed on the cathode or on the protective layer.

**12**. The organic light emitting diode display of claim **1**, wherein the power line includes a low resistance material.

**13**. The organic light emitting diode display of claim **1**, further comprising an organic light emitting layer in the organic light emitting diode and divided by the first barrier, the organic light emitting layer exposing a portion of the auxiliary electrode,

wherein on the auxiliary electrode, the cathode is horizontally extended further than the organic light emitting layer.

**14**. The organic light emitting diode display of claim **1**, wherein the cathode and the protective layer each have a portion sequentially stacked on the first barrier.

**15**. The organic light emitting diode display of claim **1**, wherein the conductive filler layer includes at least one of poly(3,4-ethylenedioxythiophene) (PEDOT) and an ionic liquid.

**16**. The organic light emitting diode display of claim **1**, wherein the distance between the first substrate and the second substrate is selected depending on viscosity of the conductive filler layer.

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|---|---|---|---|
| 专利名称(译) | 有机发光二极管显示器 | | |
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| 申请号 | US16/106927 | 申请日 | 2018-08-21 |
| [标]申请(专利权)人(译) | 乐金显示有限公司 | | |
| 申请(专利权)人(译) | LG DISPLAY CO. , LTD. | | |
| 当前申请(专利权)人(译) | LG DISPLAY CO. , LTD. | | |
| [标]发明人 | LEE JOONSUK<br>KIM SEJUNE | | |
| 发明人 | LEE, JOONSUK<br>KIM, SEJUNE | | |
| IPC分类号 | H01L27/32 H01L51/52 | | |
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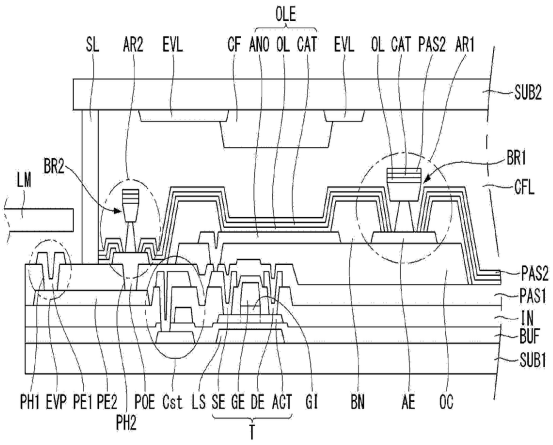
摘要(译)

公开了一种有机发光二极管显示器。有机发光二极管显示器包括：第一基板，其上各自包括有机发光二极管的像素;第二基板，包括供应有电源电压并面向第一基板的电源线;以及导电填充层，介于第一基板和第一基板之间。基板和第二基板并包括导电介质。第一基板包括辅助电极，设置在辅助电极上的第一屏障，由第一屏障分隔并暴露至少一部分辅助电极的阴极，以及设置在阴极上的保护层，由第一屏障划分，并暴露至少一部分辅助电极。阴极的一端直接接触辅助电极。